ANALOG DEVICES

Low Cost Parallel-Port 16-Bit SoundPort Stereo Codec

AD1846

FEATURES
Low Cost, Pin- and Register-Compatible Alternative to AD1848
Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Supports the Microsoft Windows Sound System*
Multiple Channels of Stereo Input and Output
Analog and Digital Signal Mixing
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
68-Lead PLCC Package
Operation from +5 V Supply
Byte-Wide Parallel Interface to ISA and EISA Buses
Supports One or Two DMA Channels and Programmed I/O

PRODUCT OVERVIEW

The Parallel-Port AD1846 SoundPort® Stereo Codec integrates key audio data conversion and control functions into a single integrated circuit. The AD1846 is intended to provide a complete, single-chip audio solution for business audio and multimedia applications requiring operation from a single +5 V supply.

*Windows Sound System is a trademark of Microsoft Corp.
SoundPort is a registered trademark of Analog Devices, Inc.

It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card. The AD1846 generates enable and direction controls for IC buffers such as the 74_245.

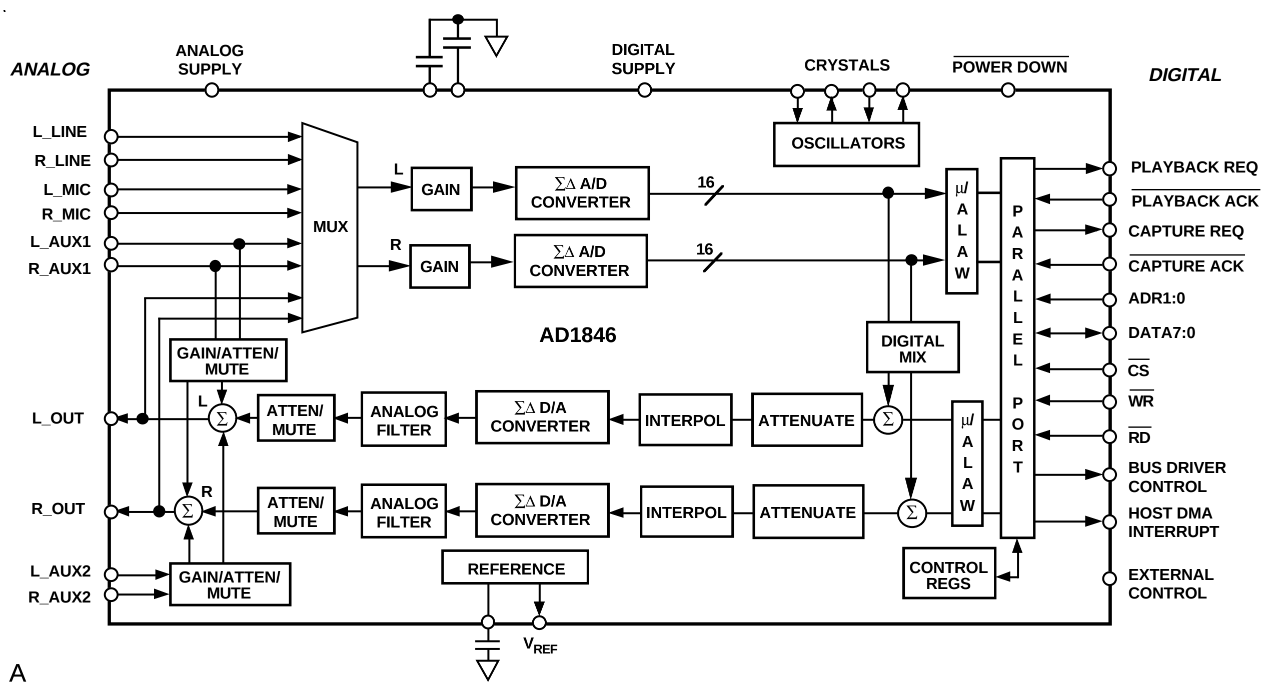
The AD1846 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. Two input control lines support mixed direct and indirect addressing of twenty-one internal control registers over this asynchronous interface.

External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. DAC dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals.

The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Inputs to the ADC can be selected from four stereo pairs of analog signals: line, microphone ("mic"), auxiliary ("aux") line #1, and post-mixed DAC output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

(Continued on page 9)

FUNCTIONAL BLOCK DIAGRAM



REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Word Rate (F_S)	48	kHz
Input Signal	1007	Hz
Analog Output Passband	20 Hz to 20 kHz	
FFT Size	4096	
V_{IH}	2.4	V
V_{IL}	0.8	V
V_{OH}	2.4	V
V_{OL}	0.4	V

DAC Output Conditions
- Post-Autocalibrated
- 0 dB Attenuation
- Full Scale (0 dB)
- 16-Bit Linear Mode
- No Output Load
- Mute Off

ADC Input Conditions
- Post-Autocalibrated
- 0 dB Gain
- –1.0 dB Relative to Full Scale
- Line Input
- 16-Bit Linear Mode
- Inputs Driven with Low Impedance (≈ 50 Ω) Source

ANALOG INPUT

	Min	Typ	Max	Units
Full Scale Input Voltage (RMS Values Assume Sine Wave Input)				
Line		1		V rms
	2.5	2.8	3.1	V p-p
Mic		1		V rms
MGE = 0	2.5	2.8	3.1	V p-p
MGE = 1	0.29	0.36	0.43	V p-p
Input Impedance	100			kΩ
Input Capacitance			15	pF

PROGRAMMABLE GAIN AMPLIFIER—ADC

	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested)	1.0	1.5	2.0	dB
PGA Gain Range Span	21.0	22.5	24.0	dB

AUXILIARY INPUT ANALOG AMPLIFIERS/ATTENUATORS

	Min	Typ	Max	Units
Step Size (+12 dB to –28.5 dB, Referenced to DAC Full Scale)	1.3	1.5	1.7	dB
(–30 dB to –34.5 dB, Referenced to DAC Full Scale)	1.0	1.5	2.0	dB
Auxiliary Gain/Attenuation Range Span	45.5	46.5	47.5	dB
Auxiliary Input Impedance*	10			kΩ

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

	Min	Max	Units
Passband	0	$0.4 \times F_S$	Hz
Passband Ripple		±0.1	dB
Transition Band	$0.4 \times F_S$	$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$	∞	Hz
Stopband Rejection	74		dB
Group Delay		$30/F_S$	
Group Delay Variation Over Passband		0.0	µs

ANALOG-TO-DIGITAL CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	70	75		dB
THD+N (Referenced to Full Scale)			0.02	%
		–72	–70	dB
Signal-to-Intermodulation Distortion		83		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)			–80	dB
Line to MIC (Input LINE, Ground and Select MIC, Read Both Channels)			–80	dB
Line to AUX1			–80	dB
Line to AUX2			–80	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			12	mV

DIGITAL-TO-ANALOG CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	80	83		dB
THD+N (Referenced to Full Scale)			0.02	%
		–73	–70	dB
Signal-to-Intermodulation Distortion		86		dB
Gain Error (Full-Scale Span Relative to Nominal Output Voltage)			±10	%
Interchannel Gain Mismatch (Difference of L and R Gain Errors)			±0.5	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			–80	dB
Total Out-of-Band Energy* (Measured from $0.6 \times F_S$ to 96 kHz)			–50	dB
Audible Out-of-Band Energy* (Measured from $0.6 \times F_S$ to 20 kHz, Tested at 5.5 kHz)			–70	dB

*Guaranteed Not Tested.
Specifications subject to change without notice.

DAC ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to –60 dB) (Tested at Steps 0 dB, –19.5 dB and –60 dB)	1.3	1.5	1.7	dB
Step Size (–60 dB to –94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation Range Span*	93.5	94.5	95.5	dB

ANALOG OUTPUT

	Min	Typ	Max	Units
Full-Scale Output Voltage		0.707		V rms
	1.8	2.0	2.2	V p-p
Output Impedance*			600	Ω
External Load Impedance	10			kΩ
Output Capacitance*			15	pF
External Load Capacitance			100	pF
V_{REF}	2.00	2.25	2.50	V
V_{REF} Current Drive		100		µA
V_{REF} Output Impedance		4		kΩ
Mute Attenuation of 0 dB Fundamental* (OUT)			–80	dB
Mute Click (|Muted Output Minus Unmuted Midscale DAC Output|)			5	mV

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
Peak-to-Peak Frequency Response Ripple* (Line In to Line Out)			1.0	dB
Differential Nonlinearity*			±1	Bit
Phase Linearity Deviation*			5	Degrees

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.4	(V_{DD}) + 0.3	V
XTAL1/2I	2.4	(V_{DD}) + 0.3	V
Low Level Input Voltage (V_{IL})	–0.3	0.8	V
High Level Output Voltage (V_{OH}) at I_{OH} = –2 mA	2.4		V
Low Level Output Voltage (V_{OL}) at I_{OL} = 2 mA		0.4	V
Input Leakage Current (GO/NOGO Tested)	–10	10	µA
Output Leakage Current (GO/NOGO Tested)	–10	10	µA

DIGITAL MIX ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to –94 dB) (Tested at Steps 0 dB, –19.5 dB)	1.0	1.5	2.0	dB
Output Attenuation Range Span*	–93.5		95.5	dB

*Guaranteed, not tested.

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

	Min	Max	Units
$\overline{WR}/\overline{RD}$ Strobe Width (t_{STW})	130		ns
$\overline{WR}/\overline{RD}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{BWND})	140		ns
Write Data Setup to $\overline{WR}$ Rising (t_{WDSU})	10		ns
$\overline{RD}$ Falling to Valid Read Data (t_{RDDV})	20	40	ns
$\overline{CS}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{CSSU})	10		ns
$\overline{CS}$ Hold from $\overline{WR}/\overline{RD}$ Rising (t_{CSHD})	0		ns
Adr Setup to $\overline{WR}/\overline{RD}$ Falling (t_{ADSU})	10		ns
Adr Hold from $\overline{WR}/\overline{RD}$ Rising (t_{ADHD})	10		ns
$\overline{DAK}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{SUDK1})	60		ns
$\overline{DAK}$ Falling to $\overline{WR}/\overline{RD}$ Rising (t_{SUDK2})	0		ns
$\overline{DAK}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{DKSU})	25		ns
Data Hold from $\overline{RD}$ Rising (t_{DHD1})	0	20	ns
Data Hold from $\overline{WR}$ Rising (t_{DHD2})	15		ns
DRQ Hold from $\overline{WR}/\overline{RD}$ Falling (t_{DRHD})	0	30	ns
$\overline{DAK}$ Hold from $\overline{WR}$ Rising (t_{DKHDa})	10		ns
$\overline{DAK}$ Hold from $\overline{RD}$ Rising (t_{DKHDb})	10		ns
$\overline{DBEN}$/DBDIR Delay from $\overline{WR}/\overline{RD}$ Falling (t_{DBDL})	0	20	ns

POWER SUPPLY

	Min	Max	Units
Power Supply Range – Analog	4.75	5.25	V
Power Supply Range – 5 V Digital	4.75	5.25	V
Power Supply Current – 5 V Operating (5 V Supplies)		120	mA
Analog Supply Current – 5 V Operating		65	mA
Digital Supply Current – 5 V Operating		55	mA
Digital Power Supply Current – Power Down		0.5	mA
Analog Power Supply Current – Power Down		0.5	mA
Power Dissipation – 5 V Operating (Current • Nominal Supplies)		600	mW
Power Dissipation – Power Down (Current • Nominal Supplies)		5	mW
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)	40		dB

CLOCK SPECIFICATIONS*

	Min	Max	Units
Input Clock Frequency		27	MHz
Recommended Clock Duty Cycle Tolerance		±10	%
Initialization Time			
16.9344 MHz Crystal Selected		70	ms
24.576 MHz Crystal Selected		90	ms

*Guaranteed, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	–0.3	6.0	V
Analog (V_{CC})	–0.3	6.0	V
Input Current			
(Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	(V_{CC}) + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	(V_{DD}) + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

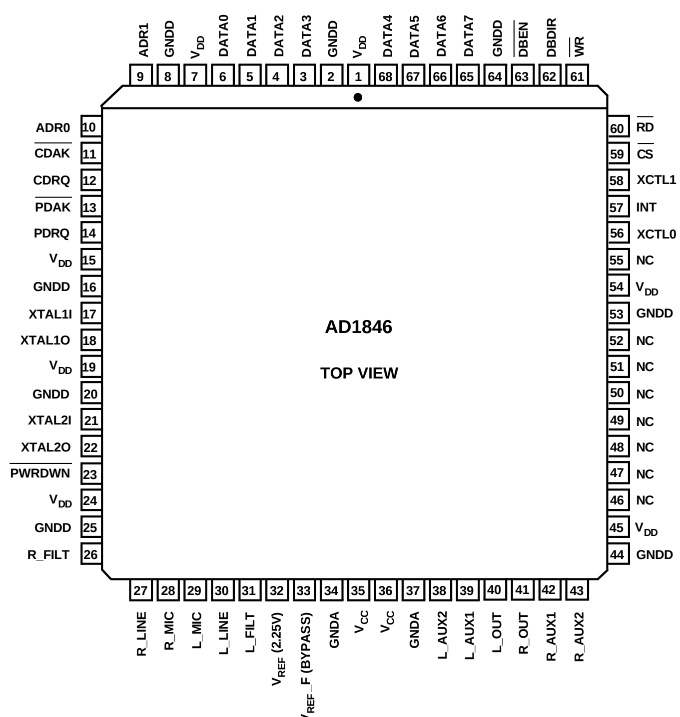
Model	Temperature Range	Package Description
AD1846JP	0°C to +70°C	68-Lead PLCC

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1846 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



68-Lead Plastic Leaded Chip Carrier Pinout



NC = NO CONNECT

PIN DESCRIPTION

Parallel Interface

Pin Name	PLCC	I/O	Description
CDRQ	12	O	Capture Data Request. The assertion of this signal indicates that the Codec has a captured audio sample from the ADC ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.
$\overline{\text{CDAK}}$	11	I	Capture Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.
PDRQ	14	O	Playback Data Request. The assertion of this signal indicates that the Codec is ready for more DAC playback data. The signal will remain asserted until all the bytes needed for a playback sample have been transferred.
$\overline{\text{PDAK}}$	13	I	Playback Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.
ADR1:0	9 & 10	I	Codec Addresses. These address pins are asserted by the Codec interface logic during a control register/PIO access. The state of these address lines determine which register is accessed.
$\overline{\text{RD}}$	60	I	Read Command Strobe. This active LO signal defines a read cycle from the Codec. The cycle may be a read from the control/PIO registers, or the cycles could be a read from the Codec's DMA sample registers.
$\overline{\text{WR}}$	61	I	Write Command Strobe. This active LO signal indicates a write cycle to the Codec. The cycle may be a write to the control/PIO registers, or the cycle could be a write to the Codec's DMA sample registers.
$\overline{\text{CS}}$	59	I	AD1846 Chip Select. The Codec will not respond to any control/PIO cycle accesses unless this active LO signal is LO. This signal is ignored during DMA transfers.
DATA7:0	3–6 & 65–68	I/O	Data Bus. These pins transfer data and control information between the Codec and the host.
$\overline{\text{DBEN}}$	63	O	Data Bus Enable. This pin enables the external bus drivers. This signal is normally HI. For control register/PIO cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ OR $\overline{\text{RD}}$) AND $\overline{\text{CS}}$ For DMA cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ OR $\overline{\text{RD}}$) AND ($\overline{\text{PDAK}}$ OR $\overline{\text{CDAK}}$)
DBDIR	62	O	Data Bus Direction. This pin controls the direction of the data bus transceiver. HI enables writes from the host to the AD1846; LO enables reads from the AD1846 to the host bus. This signal is normally HI. For control register/PIO cycles, DBDIR = $\overline{\text{RD}}$ AND $\overline{\text{CS}}$ For DMA cycles, DBDIR = $\overline{\text{RD}}$ AND ($\overline{\text{PDAK}}$ OR $\overline{\text{CDAK}}$)

Analog Signals

Pin Name	PLCC	I/O	Description
L_LINE	30	I	Left Line Input. Line level input for the left channel.
R_LINE	27	I	Right Line Input. Line level input for the right channel.
L_MIC	29	I	Left Microphone Input. Microphone input for the left channel. This signal can be either line level or –20 dB from line level.
R_MIC	28	I	Right Microphone Input. Microphone input for the right channel. This signal can be either line level or –20 dB from line level.
L_AUX1	39	I	Left Auxiliary #1 Line Input
R_AUX1	42	I	Right Auxiliary #1 Line Input
L_AUX2	38	I	Left Auxiliary #2 Line Input
R_AUX2	43	I	Right Auxiliary #2 Line Input
L_OUT	40	O	Left Line Level Output
R_OUT	41	O	Right Line Level Output

Miscellaneous

Pin Name	PLCC	I/O	Description
XTAL1I	17	I	24.576 MHz Crystal #1 Input
XTAL1O	18	O	24.576 MHz Crystal #1 Output
XTAL2I	21	I	16.9344 MHz Crystal #2 Input
XTAL2O	22	O	16.9344 MHz Crystal #2 Output
$\overline{\text{PWRDWN}}$	23	I	Power-Down Signal. Active LO control places AD1846 in its lowest power consumption mode. All sections of the AD1846, including the digital interface, are shut down and consume minimal power.
INT	57	O	Host Interrupt Pin. This signal is used to notify the host that the DMA Current Count Register has underflowed.
XCTL1:O	56 & 58	O	External Control. These signals reflect the current status of register bits inside the AD1846. They can be used for signaling or to control external logic. XLTL1 and XLTL0 are open-drain outputs.
V_{REF}	32	O	Voltage Reference. Nominal 2.25 volt reference available externally for dc-coupling and level-shifting. V_{REF} should not be used where it will sink or source current.
V_{REF}_F	33	I	Voltage Reference Filter. Voltage reference filter point for external bypassing only.
L_FILT	31	I	Left Channel Filter Input. This pin requires a 1.0 µF capacitor to analog ground for proper operation.
R_FILT	26	I	Right Channel Filter Input. This pin requires a 1.0 µF capacitor to analog ground for proper operation.
NC	46–52, 55		No Connect. Do not connect.

Power Supplies

Pin Name	PLCC	I/O	Description
V_{CC}	35 & 36	I	Analog Supply Voltage (+5 V)
GNDA	34 & 37	I	Analog Ground
V_{DD}	1, 7, 15, 19, 24, 45, 54	I	Digital Supply Voltage (+5 V)
GNDD	2, 8, 16, 20, 25, 44, 53, 64	I	Digital Ground

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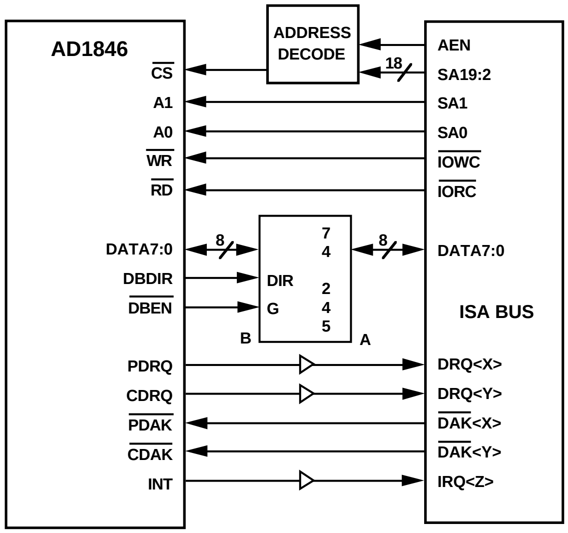


Figure 1. Interface to ISA Bus

The pair of 16-bit outputs from the ADCs is available over a byte-wide bidirectional interface that also supports 16-bit digital input to the DACs and control information. The AD1846 can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit µ-law or A-law companded digital data.

The $\Sigma\Delta$ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantization noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output.

AUDIO FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1846 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1846 SoundPort Stereo Codec accepts stereo line-level and mic-level inputs. LINE, MIC, and AUX1 inputs and post-mixed DAC output analog stereo signals are multiplexed to the internal programmable gain amplifier (PGA) stage.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left channel inputs appearing at both channel outputs.

Analog Mixing

AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary analog input can be independently gained/attenuated from +12 dB to –34.5 dB in –1.5 dB steps or completely muted. The post mixed DAC output is available on OUT externally and as an input to the ADCs.

Even if the AD1846 is not playing back data from its DACs, the analog mix function can still be active.

Analog-to-Digital Datapath

The AD1846 $\Sigma\Delta$ ADCs incorporate a fourth order modulator. A single pole of passive filtering is all that is required for anti-aliasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include linear phase digital decimation filters that low-pass filter the input to $0.4 \times F_S$. ("F_S'' is the word rate or "sampling frequency"). ADC input overrange conditions will cause bits to be set that can be read.

Each channel of the mic inputs can be amplified digitally by +18 dB to compensate for the voltage swing differences between line levels and typical condenser microphone levels. This +18 dB digital gain is enabled with the same control bits (LMGE and RMGE) as the +20 dB analog gain in the AD1848.

Digital-to-Analog Datapath

The $\Sigma\Delta$ DACs contain a programmable attenuator and a low-pass digital interpolation filter. The anti-imaging interpolation filter oversamples by 64 and digitally filters the higher frequency images. The attenuator allows independent control of each DAC channel from 0 dB to –94.5 dB in 1.5 dB steps plus full mute. The DACs' $\Sigma\Delta$ noise shapers also oversample by 64 and convert the signal to a single bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output. No external components are required. Phase linearity at the analog output is achieved by internally compensating for the group delay variation of the analog output filters.

Changes in DAC output attenuation take effect only on zero crossings, thereby eliminating "zipper" noise. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 8 milliseconds at a 48 kHz sampling rate and 48 milliseconds at an 8 kHz sampling rate. (Time out [ms] $\approx 384/F_S$ [kHz].)

Digital Mixing

Stereo digital output from the ADCs can be mixed digitally with the input to the DACs. Digital output from the ADCs going out of the data port is unaffected by the digital mix. Along the digital mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally the AD1846 always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixty-four steps of –1.5 dB attenuation are supported to –94.5 dB. The digital mix datapath can also be completely muted, preventing any mixing of the analog input with the digital input. Note that the level of the mixed signal is also a function of the input PGA settings, since they affect the ADCs' output.

The attenuated digital mix data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators.

In case the AD1846 is capturing data but ADC output data is not removed in time ("ADC overrun"), then the last sample captured before overrun will be used for the digital mix. In case the AD1846 is playing back data hut input digital DAC data fails to arrive in time ("DAC underrun"), then a midscale zero will be added to the digital mix data.

Analog Outputs

A stereo line level output is available at external pins. Each channel of this output can be independently muted. When muted, the outputs will settle to a dc value near V_{REF}, the midscale reference voltage.

Digital Data Types

The AD1846 supports four data types: 16-bit twos-complement linear PCM, eight-bit unsigned linear PCM, companded µ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. Stereo data is always transferred in the left-right order. All data formats that are less than 16 bits are properly aligned to insure the utilization of full system resolution.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded µ-law and A-law data formats use nonlinear coding with less precision for large amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether µ-law or A-law was specified in the Codec's internal registers. Note that when µ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits.

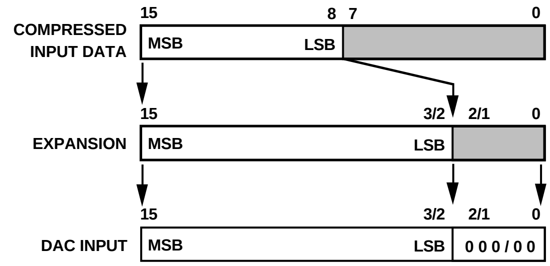


Figure 2. A-Law or µ-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified.

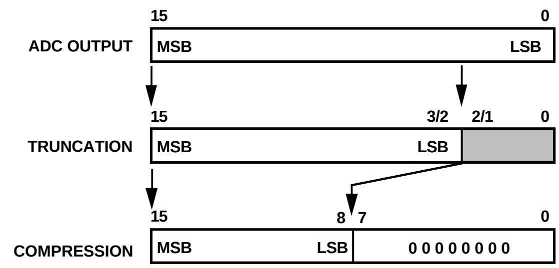


Figure 3. A-Law or µ-Law Compression

Note that all format conversions take place at input or output. Internally, the AD1846 always uses 16-bit linear PCM representations to maintain maximum precision.

Power Supplies and Voltage Reference

The AD1846 operates from +5 V power supplies. Independent analog and digital supplies are recommended for optimal performance though excellent results can be obtained in single supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (V_{REF}). The reference output can be used for biasing op amps used in dc coupling. The internal reference must be externally bypassed to analog ground at the V_{REF}_F pin.

Clocks and Sample Rates

The AD1846 operates from external crystals. Two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1846, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them the following sample rates are divided down: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz.

CONTROL REGISTERS

Control Register Architecture

The AD1846 SoundPort Stereo Codec accepts both data and control information through its byte-wide parallel port. Indirect addressing minimizes the number of external pins required to access all 21 of its byte-wide internal registers. Only two external address pins, ADR1:0, are required to accomplish all data and control transfers. These pins select one of five direct registers. (ADR1:0 = 3 addresses two registers, depending on whether the transfer is a playback or a capture.)

ADR1:0	Register Name
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Registers

Figure 4. Direct Register Map

A write to or a read from the Indexed Data Register will access the indirect register which is indexed by the value most recently written to the Index Address Register. The Status Register and the PIO Data Register are always accessible directly, without indexing. The 16 indirect registers are indexed in Figure 5.

Index	Register Name
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left Output Control
7	Right Output Control
8	Clock and Data Format
9	Interface Configuration
10	Pin Control
11	Test and Initialization
12	Miscellaneous Information
13	Digital Mix
14	Upper Base Count
15	Lower Base Count

Figure 5. Indirect Register Map

A detailed map of all direct and indirect register contents is summarized for reference as follows:

Direct Registers:

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	INIT	MCE	TRD	res	IXA3	IXA2	IXA1	IXA0
1	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers:

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0
2	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0
3	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0
4	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0
5	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0
6	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8	res	FMT	C/L	S/M	CFS2	CFS1	CFS0	CSS
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	res	res	res	res	IEN	res
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	res	res	res	res	ID3	ID2	ID1	ID0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

Figure 6. Register Summary

Note that the only sticky bit in any of the AD1846 control registers is the interrupt (INT) bit. All other bits change with every sample period.

Direct Control Register Definitions

Index Register (ADR1:0 = 0)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	INIT	MCE	TRD	res	IXA3	IXA2	IXA1	IXA0

IXA3:0 Index Address. These bits define the address of the AD1846 register accessed by the Indexed Data Register. These bits are read/write.

res Reserved for future expansion. Always write a zero to this bit.

TRD Transfer Request Disable. This bit, when set, causes all data transfers to cease when the Interrupt Status (INT) bit of the Status Register is set.

0 Transfers Enabled During Interrupt. PDRQ and CDRQ pin outputs are generated uninhibited by interrupts. DMA Current Counter Register decrements with every sample period when either PEN or CEN are enabled.

1 Transfers Disabled By Interrupt. PDRQ and CDRQ pin outputs are generated only if INT bit is 0 (when either PEN or CEN, respectively, are enabled). Any pending playback or capture requests are allowed to complete at the time when TRD is set. After pending requests complete, midscale inputs will be internally generated for the DACs, and the ADC output buffer will contain the last valid output. Clearing the sticky INT bit (or the TRD bit) will cause the resumption of playback and/or capture requests (presuming PEN and/or CEN are enabled). The DMA Current Counter Register will not decrement while both the TRD bit is set and the INT bit is a one.

MCE Mode Change Enable. This bit must be set whenever the current functional mode of the AD1846 is changed. Specifically, the Clock and Data Format and Interface Configuration registers cannot be changed unless this bit is set. The exceptions are CEN and PEN in the Interface Configuration which can be changed "on-the-fly." MCE should be cleared at the completion of the desired register changes. The DAC outputs are automatically muted when the MCE bit is set. After MCE is cleared, the DAC outputs will be restored to the state specified by the LDM and RDM mute bits.

Both ADCs and DACs are automatically muted for approximately 128 sample cycles after exiting the MCE state to allow the reference and all filters to settle. The ADCs will produce midscale values; the DACs' analog output will be muted. All converters are internally operating during these ≈128 sample cycles, and the AD1846 will expect playback data and will generate (midscale) capture data. Note that the autocalibrate-in-process (ACI) bit will be set on exit from the MCE state regardless of whether or not ACAL was set. ACI will remain HI for these ≈128 sample cycles; system software should poll this bit rather than count cycles.

Special sequences must be followed if autocalibrate (ACAL) is set or sample rates are changed (CFS2:0 and or CSS) during mode change enable. See the "Autocalibration" and "Changing Sample Rates" sections below.

INIT AD1846 Initialization. This bit is set when the AD1846 is in a state which cannot respond to parallel bus cycles. This bit is read only.

Immediately after reset and once the AD1846 has left the INIT state, the initial value of this register will be "0100 0000 (40h)." During AD1846 initialization, this register cannot be written to and will always read "100x 0000 (80h)."

Indexed Data Register (ADR1:0 = 1)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0

IXD7:0 Indexed Register Data. These bits contain the contents of the AD1846 register referenced by the Indexed Data Register.

During AD1846 initialization, this register cannot be written to and will always read as "1000 0000 (80h)."

Status Register (ADR1:0 = 2)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT

INT Interrupt Status. This sticky bit (the only one) indicates the status of the interrupt logic of the AD1846. This bit is cleared by any host write of any value to this register. The IEN bit of the Pin Control Register determines whether the state of this bit is reflected on the INT pin of the AD1846. The only interrupt condition supported by the AD1846 is generated by the underflow of the DMA Current Count Register.

0 Interrupt pin inactive

1 Interrupt pin active

PRDY Playback Data Register Ready. The PIO Playback Data Register is ready for more data. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read only.

0 DAC data is still valid. Do not overwrite.

1 DAC data is stale. Ready for next host data write value.

PL/R Playback Left/Right Sample. This bit indicates whether the PIO playback data needed is for the right channel DAC or left channel DAC. This bit is read only.

0 Right channel needed

1 Left channel or mono

PU/L Playback Upper/Lower Byte. This bit indicates whether the PIO playback data needed is for the upper or lower byte of the channel. This bit is read only.

0 Lower byte needed

1 Upper byte needed or any 8-bit mode

SOUR Sample Over/Underrun. This bit indicates that the most recent sample was not serviced in time and therefore either a capture overrun (COR) or playback underrun (PUR) has occurred. The bit indicates an overrun for ADC capture and an underrun for DAC playback. If both capture and playback are enabled, the source which set this bit can be determined by reading COR and PUR. This bit changes on a sample-by-sample basis. This bit is read only.

CRDY Capture Data Ready. The PIO Capture Data Register contains data ready for reading by the host. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read only.

0 ADC data is stale. Do not reread the information.

1 ADC data is fresh. Ready for next host data read.

CL/R Capture Left/Right Sample. This bit indicates whether the PIO capture data waiting is for the right channel ADC or left channel ADC. This bit is read only.

0 Right channel

1 Left channel or mono

CU/L Capture Upper/Lower Byte. This bit indicates whether the PIO capture data ready is for the upper or lower byte of the channel. This bit is read only.

0 Lower byte ready

1 Upper byte ready or any 8-bit mode

The PRDY, CRDY, and INT bits of this status register can change asynchronously to host accesses. The host may access this register while the bits are transitioning. The host read may return a zero value just as these bits are changing, for example. A “1” value would not be read until the next host access.

This registers’s initial state after reset is “1100 1100.”

PIO Data Registers (ADR1:0 = 3)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The PIO Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0).

During AD1846 initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000 (80h)."

CD7:0 PIO Capture Data Register. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, the state machine and status register will point to the first byte of the sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

PD7:0 PIO Playback Data Register. This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Indirect Control Register Definitions

The following control registers are accessed by writing index values to IXA3:0 in the Index Address Register (ADR1:0 = 0) followed by a read/write to the Indexed Data Register (ADR1:0 = 1).

Left Input Control (IXA3:0 = 0)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0

LIG3:0 Left input gain select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

LMGE Left Input Microphone Gain Enable. Setting this bit will enable the +18 dB digital gain of the left mic input signal.

LSS1:0 Left Input Source Select. These bits select the input source for the left gain stage preceding the left ADC.

- 0 Left Line Source Selected
- 1 Left Auxiliary 1 Source Selected
- 2 Left Microphone Source Selected
- 3 Left Line Post-Mixed DAC Output Source Selected

This register's initial state after reset is "000x 0000."

Right Input Control (IXA3:0 = 1)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0

RIG3:0 Right Input Gain Select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

RMGE Right Input Microphone Gain Enable. Setting this bit will enable the +18 dB digital gain of the right mic input signal.

RSS1:0 Right Input Source Select. These bits select the input source for the right channel gain stage preceding the right ADC.

- 0 Right Line Source Selected
- 1 Right Auxiliary 1 Source Selected
- 2 Right Microphone Source Selected
- 3 Right Post-Mixed DAC Output Source Selected

This register's initial state after reset is "000x 0000."

Left Auxiliary #1 Input Control (IXA3:0 = 2)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
2	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0

LX1A4:0 Left Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents –1.5 dB. LX1A4:0 = 0 produces a +12 dB gain. LX1A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is –34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX1 Left Auxiliary #1 Mute. This bit, when set, will mute the left channel of the Auxiliary #1 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Right Auxiliary #1 Input Control (IXA3:0 = 3)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0

RX1A4:0 Right Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents –1.5 dB. RX1A4:0 = 0 produces a +12 dB gain. RX1A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is –34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX1 Right Auxiliary #1 Mute. This bit, when set, will mute the right channel of the Auxiliary #1 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Left Auxiliary #2 Input Control (IXA3:0 = 4)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
4	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0

LX2A4:0 Left Auxiliary Input #2 Attenuate Select. The least significant bit of this gain/attenuate select represents –1.5 dB. LX2A4:0 = 0 produces a +12 dB gain. LX2A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is –34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX2 Left Auxiliary #2 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #2 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Right Auxiliary #2 Input Control (IXA3:0 = 5)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
5	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0

RX2A4:0 Right Auxiliary Input #2 Attenuate Select. The least significant bit of this gain/attenuate select represents –1.5 dB. RX2A4:0 = 0 produces a +12 dB gain. RX2A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is –34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX2 Right Auxiliary #2 Mute. This bit, when set, will mute the right channel of the Auxiliary #2 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Left DAC Control (IXA3:0 = 6)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
6	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5:0 Left DAC Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. LDA5:0 = 0 produces a 0 dB attenuation. Maximum attenuation is –94.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

LDM Left DAC Mute. This bit, when set to 1, will mute the left DAC output. Auxiliary inputs are muted independently with the Left Auxiliary Input Control Registers. This bit is set to "1" after reset.

This register's initial state after reset is "1x00 0000."

Right DAC Control (IXA3:0 = 7)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
7	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5:0 Right DAC Attenuate Select. The least significant bit of this attenuate select represents –1.5 dB. RDA5:0 = 0 produces 0 dB attenuation. Maximum attenuation is –94.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

RDM Right DAC Mute. This bit, when set to 1, will mute the right DAC output. Auxiliary inputs are muted independently with the Right Auxiliary Input Control Registers. This bit is set to "1" after reset.

This register's initial state after reset is "1x00 0000."

Clock and Data Format Register (IXA3:0 = 8)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
8	res	FMT	C/L	S/M	CFS2	CFS1	CFS0	CSS

The contents of the Clock and Data Format Register cannot be changed except when the AD1846 is in Mode Change Enable (MCE) state. Write attempts to this register when the AD1846 is not in the MCE state will not be successful.

CSS Clock Source Select. These bits select the crystal clock source which will be used for the audio sample rates.

0 XTAL1 (24.576 MHz)

1 XTAL2 (16.9344 MHz)

CFS2:0 Clock Frequency Divide Select. These bits select the audio sample rate frequency. The actual audio sample rate depends on which crystal clock source is selected and the frequency of that source.

CFS	Divide Factor	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0	3072	8.0 kHz	5.5125 kHz
1	1536	16.0 kHz	11.025 kHz
2	896	27.42857 kHz	18.9 kHz
3	768	32.0 kHz	22.05 kHz
4	448	Not Supported	37.8 kHz
5	384	Not Supported	44.1 kHz
6	512	48.0 kHz	33.075 kHz
7	2560	9.6 kHz	6.615 kHz

Note that the AD1846's internal oscillators can be driven by external clock sources at the crystal input pins. If an external clock source is applied, it will be divided down by the selected Divide Factor. It need not be at the recommended crystal frequencies.

S/M Stereo/Mono Select. This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

0 Mono

1 Stereo

C/L Companded/Linear Select. This bit selects between a linear digital representation of the audio signal or a nonlinear, companded format for all input and output data. The type of linear PCM or the type of companded format is defined by the FMT bits.

0 Linear PCM

1 Companded

FMT Format Select. This bit defines the format for all digital audio input and outputs based on the state of the C/L bit.

	Linear PCM (C/L = 0)	Companded (C/L = 1)
0	8-bit Unsigned PCM	8-bit µ-law Companded
1	16-bit Twos-Complement PCM	8-bit A-law Companded

res Reserved for future expansion. Always write a zero to this bit.

This register's initial state after reset is "x000 0000."

Interface Configuration Register (IXA3:0 = 9)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

The contents of the Interface Configuration Register cannot be changed except when the AD1846 is in Mode Change Enable (MCE) state. Write attempts to this register when the AD1846 is not in the MCE state will not be successful. PEN and CEN are exceptions; these bits may always be written.

PEN Playback Enable. This bit will enable the playback of data in the format selected. The AD1846 will generate PDRQ and respond to $\overline{\text{PDAK}}$ signals when this bit is enabled and PPIO = 0. If PPIO = 1, this bit enables Programmed I/O (PIO) playback mode. PEN may be set and reset without setting the MCE bit.

0 Playback disabled (PDRQ and PIO Playback Data Register inactive)

1 Playback enabled

CEN Capture Enable. This bit will enable the capture of data in the format selected. The AD1846 will generate CDRQ and respond to $\overline{\text{CDAK}}$ signals when this bit is enabled and CPIO = 0. If CPIO = 1, this bit enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 Capture disabled (CDRQ and PIO Capture Data Register inactive)

1 Capture enabled

SDC Single DMA Channel. This bit will force both capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be LO. This bit will allow the AD1846 to be used with only one DMA channel. Simultaneous capture and playback cannot occur in this mode. Should both capture and playback be enabled (CEN = PEN = 1) in the mode, only playback will occur. See "Data and Control Transfers" for further explanation.

0 Dual DMA channel mode

1 Single DMA channel mode

ACAL Autocalibrate Enable. This bit determines whether the AD1846 performs an autocalibrate whenever the $\overline{\text{PWRDWN}}$ pin is deasserted or from the Mode Change Enable (MCE) bit being reset. ACAL is normally set. See "Autocalibration" below for a description of a complete autocalibration sequence.

0 No autocalibration

1 Autocalibration after power down/reset or mode change

res Reserved for future expansion. Always write zeros to these bits.

PPIO Playback PIO Enable. This bit determines whether the playback data is transferred via DMA or PIO.

0 DMA transfers only

1 PIO transfers only

CPIO Capture PIO Enable. This bit determines whether the capture data is transferred via DMA or PIO.

0 DMA transfers only

1 PIO transfers only

This register's initial state after reset is "00xx 1000."

Pin Control Register (IXA3:0 = 10)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
10	XCTL1	XCTL0	res	res	res	res	IEN	res

res Reserved for future expansion. Always write zeros to these bits.

IEN Interrupt Enable. This bit enables the interrupt pin. The Interrupt Pin will go active HI when the number of samples programmed in the Base Count Register is reached.

0 Interrupt disabled

1 Interrupt enabled

XCTL1:0 External Control. The state of these independent bits is reflected on the respective XCTL1:0 pins of the AD1846.

0 TTL Logic LO on XCTL1:0 pins

1 TTL Logic HI on XCTL1:0 pins

This register's initial state after reset is "00xx xx0x."

Test and Initialization Register (IXA3:0 = 11)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1:0 Overrange Left Detect. These bits indicate the overrange on the left input channel. This bit changes on a sample-by-sample basis. This bit is read only.

- 0 Less than –1 dB underrange
- 1 Between –1 dB and 0 dB underrange
- 2 Between 0 dB and +1 dB overrange
- 3 Greater than +1 dB overrange

ORR1:0 Overrange Right Detect. These bits indicate the overrange on the right input channel. This bit changes on a sample-by-sample basis. This bit is read only.

- 0 Less than –1 dB underrange
- 1 Between –1 dB and 0 dB underrange
- 2 Between 0 dB and +1 dB overrange
- 3 Greater than +1 dB overrange

DRS Data Request Status. This bit indicates the current status of the PDRQ and CDRQ pins of the AD1846.

- 0 CDRQ and PDRQ are presently inactive (LO)
- 1 CDRQ or PDRQ are presently active (HI)

ACI Autocalibrate-In-Progress. This bit indicates the state of autocalibration or a recent exit from Mode Change Enable (MCE). This bit is read only.

- 0 Autocalibration is not in progress
- 1 Autocalibration is in progress or MCE was exited within approximately the last 128 sample periods

PUR Playback Underrun. This bit is set when playback data has not arrived from the host in time to be played. As a result, a midscale value will be sent to the DACs. This bit changes on a sample by sample basis.

COR Capture Overrun. This bit is set when the capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample will be ignored. This bit changes on a sample by sample basis.

The occurrence of a PUR and/or COR is designated in the Status Register's Sample Overrun/Underrun (SOUR) bit. The SOUR bit is the logical OR of the COR and PUR bits. This enables a polling host CPU to detect an overrun/underrun condition while checking other status bits.

This register's initial state after reset is "0000 0000."

Miscellaneous Control Register (IXA3:0 = 12)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
12	res	res	res	res	ID3	ID2	ID1	ID0

res Reserved for future expansion. The bits are read only. Do not write to these bits.

ID3:0 AD1846 Revision ID. These four bits define the revision level of the AD1846. The AD1846 is designated ID = "1010." Revisions increment by one LSB. These bits are read only.

This register's initial state after reset is "xxxx RRRR" where RRRR = Revision ID of the silicon in use.

Digital Mix Control Register (IXA3:0 = 13)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME

DME Digital Mix Enable. This bit will enable the digital mix of the ADCs' output with the DACs' input. When enabled, the data from the ADCs are digitally mixed with other data being delivered to the DACs (regardless of whether or not playback [PEN] is enabled, i.e., set). If capture is enabled (CEN set) and there is a capture overrun (COR), then the last sample captured before overrun will be used for the digital mix. If playback is enabled (PEN set) and there is a playback underrun (PUR), then a midscale zero will be added to the digital mix data.

0 Digital mix disabled (muted)

1 Digital mix enabled

res Reserved for future expansion. Always write a zero to this bit.

DMA5:0 Digital Mix Attenuation. These bits determine the attenuation of the ADC data in mixing with the DAC input. Each attenuate step is –1.5 dB ranging to –94.5 dB.

This register's initial state after reset is "0000 00x0."

DMA BASE COUNT REGISTERS (IXA3:0 = 14 & 15)

The DMA Base Count Registers in the AD1846 simplify integration of the AD1846 in ISA systems. The ISA DMA controller requires an external count mechanism to notify the host CPU via interrupt of a full DMA buffer. The programmable DMA Base Count Registers will allow such interrupts to occur.

The Base Count Registers contain the number of sample periods which will occur before an interrupt is generated on the interrupt (INT) pin. To load, first write a value to the Lower Base Count Register. Writing a value to the Upper Base Register will cause both Base Count Registers to load into the Current Count Register. Once AD1846 transfers are enabled, each sample period the Current Count Register will decrement until zero count is reached. The next sample period after zero will generate the interrupt and reload the Current Count Register with the values in the Base Count Registers. The interrupt is cleared by a write to the Status Register.

The Host Interrupt Pin (INT) will go HI during the sample period in which the Current Count Register underflows when Interrupt Enable (IEN) is set. The Host Interrupt Pin (INT) will go LO when the Interrupt Status Bit (INT) is cleared. [Note that both the Host Interrupt Pin and the Interrupt Status Bit have the same name (INT)].

The Current Count Register is decremented every sample period when either the PEN or CEN bit is enabled and also either the Transfer Request Disable (TRD) bit or the Interrupt Status (INT) bit are zero. Note that the internal INT bit will become one on counter underflow even if the external interrupt pin is not enabled, i.e., IEN is zero. The Current Count Register is decremented in both PIO and DMA data transfer modes.

Upper Base Count Register (IXA3:0 = 14)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

UB7:0 Upper Base Count. This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters can not be read.

This register's initial state after reset is "0000 0000."

Lower Upper Base Count Register (IXA3:0 = 15)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

LB7:0 Lower Base Count. This byte is the lower byte of the base count register containing the eight least significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters cannot be read.

This register's initial state after reset is "0000 0000."

DATA AND CONTROL TRANSFERS

The AD1846 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. PIO transfers can be made on one channel while the other is performing DMA. Transfers to and from the AD1846 SoundPort Codec are asynchronous relative to the internal data conversion clock. Transfers are buffered, but the AD1846 supports no internal FIFOs. The host is responsible for providing playback data before the next digital-to-analog conversion and removing capture data before the next analog-to-digital conversion.

Data Ordering

The number of byte-wide transfers required depends on the data format selected. The AD1846 is designed for "little endian" formats in which the least significant byte (i.e., occupying the lowest memory address) gets transferred first. So 16-bit data transfers require first transferring the least significant bits 7:0 and then transferring the most significant bits 15:8, where bit 15 is the most significant bit in the word.

In addition, left channel data is always transferred before right channel data with the AD1846. The following figures should make these requirements clear.

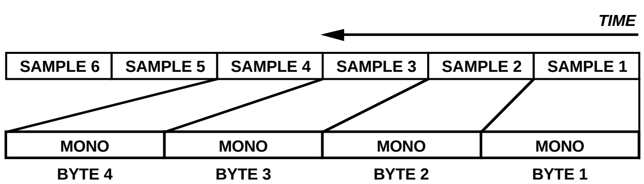


Figure 7. 8-Bit Mono Data Stream Sequencing

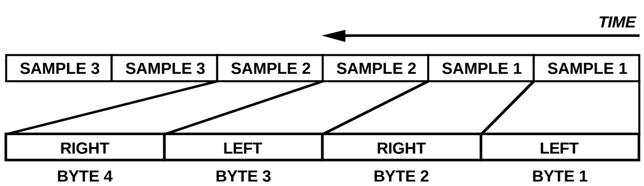


Figure 8. 8-Bit Stereo Data Stream Sequencing

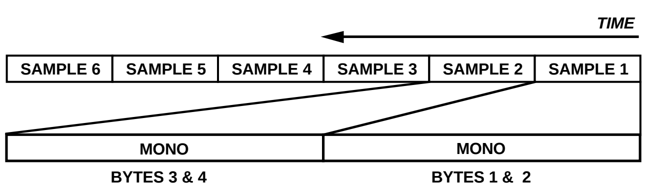


Figure 9. 16-Bit Mono Data Stream Sequencing

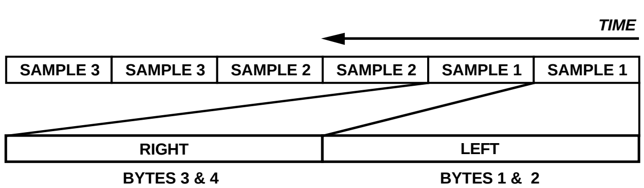


Figure 10. 16-Bit Stereo Data Stream Sequencing

Control and Programmed I/O (PIO) Transfers

This simpler mode of transfers is used both for control register accesses and programmed I/O. The 21 control and PIO data registers cannot he accessed via DMA transfers. Playback PIO is activated when both Playback Enable (PEN) is set and Playback PIO (PPIO) is set. Capture PIO is activated when both Capture Enable (CEN) is set and Capture PIO (CPIO) is set. See Figures 11 and 12 for the detailed timing of the control register/ PIO transfers. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the actual read and write cycles, respectively. The host holds $\overline{CS}$ LO during these transfers. The DMA Capture Data Acknowledge ($\overline{CDAK}$) and Playback Data Acknowledge ($\overline{PDAK}$) must be held inactive, i.e., HI.

For read/capture cycles, the AD1846 will place data on the DATA7:0 lines while the host is asserting the read strobe, $\overline{RD}$, by holding it LO. For write/playback, the host must place data on the DATA7:0 pins while strobing the $\overline{WR}$ signal LO. The AD1846 latches the write/playback data on the rising edge of the $\overline{WR}$ strobe.

When using PIO data transfers, the Status Register must be polled to determine when data should be transferred. Note that the ADC capture data will be ready (CRDY HI) from the previous sample period shortly before the DAC playback data is ready (PRDY HI) for the next sample period. The user should not wait for both ADCs and DACs to become ready before initiating data transfers. Instead, as soon as capture data is ready, it should be read; as soon as the DACs are ready, playback data should he written.

Values written to the XCTL1:0 bits in the Pin Control Register (IA3:0 = 10) will be reflected in the state of the XCTL1:0 external output pins. This feature allows a simple method for signaling or software control of external logic. Changes in state of the external XCTL pins will occur within one sample period. Because their change is referenced to the internal sample clock, no useful timing diagram can be constructed.

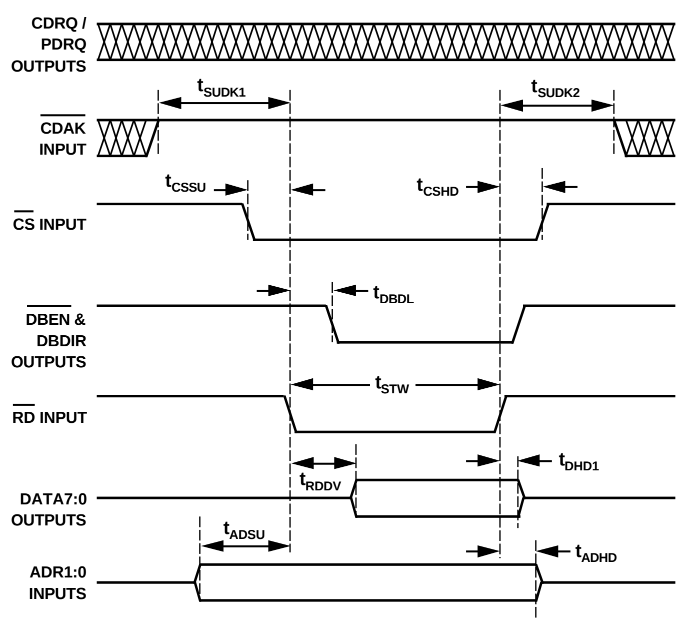


Figure 11. Control Register/PIO Read Cycle

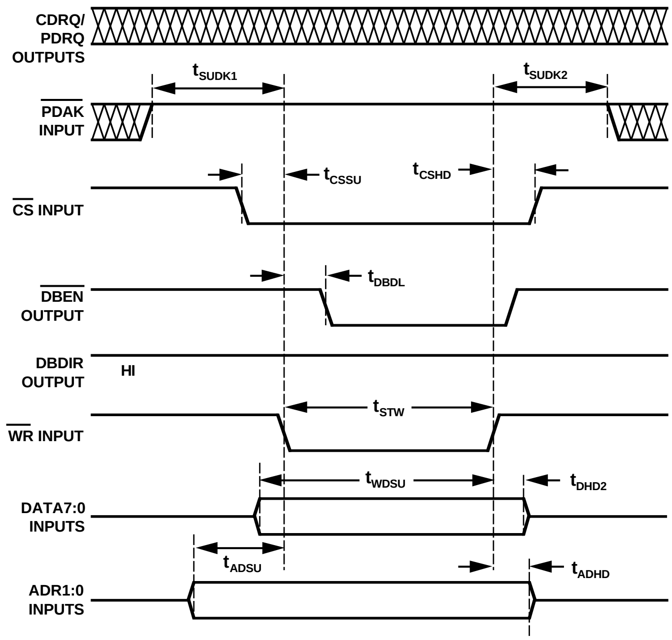


Figure 12. Control Register/PIO Write Cycle

Direct Memory Access (DMA) Transfers

The second type of bus cycle supported by the AD1846 are DMA transfers. Both dual channel and single channel DMA operations are supported. To enable Playback DMA transfers, playback enable (PEN) must be set and PPIO cleared. To enable Capture DMA transfers, capture enable (CEN) must be set and CPIO cleared. During DMA transfers, the AD1846 asserts HI the Capture Data Request (CDRQ) or the Playback Data Request (PDRQ) followed by the host's asserting LO the DMA Capture Data Acknowledge ($\overline{\text{CDAK}}$) or Playback Data Acknowledge ($\overline{\text{PDAK}}$), respectively. The host's asserted Acknowledge signals cause the AD1846 to perform DMA transfers. The input address lines, ADR1:0, are ignored. Data is transferred between the proper internal sample registers.

The read strobe ($\overline{\text{RD}}$) and write strobe ($\overline{\text{WR}}$) delimit valid data for DMA transfers. Chip select ($\overline{\text{CS}}$) is a "don't care"; its state is ignored by the AD1846.

The AD1846 asserts the Data Request signals, CDRQ and PDRQ, at the rate of once per sample period. PDRQ is asserted near the beginning of an internal sample period and CDRQ is asserted late in the same period to maximize the available processing time. Once asserted, these signals will remain active HI until the corresponding DMA cycle occurs with the host's Data Acknowledge signals. The Data Request signals will be deasserted after the falling edge of the *final* $\overline{\text{RD}}$ or WD strobe in the transfer of a sample, which typically consists of multiple bytes. See "Data Ordering" above for a definition of "sample."

DMA transfers may he independently aborted by resetting the Capture Enable (CEN) and/or Playback Enable (PEN) bits in the Interface Configuration Register. The current capture sample transfer will be completed if a capture DMA is terminated. The current playback sample transfer must be completed if a playback DMA is terminated. If CDRQ and/or PDRQ are asserted HI while the host is resetting CEN and/or PEN, the request must be acknowledged. The host must assert $\overline{\text{CDAK}}$ and/or $\overline{\text{PDAK}}$ LO and complete a final sample transfer.

Single-Channel DMA

Single-Channel DMA mode allows the AD1846 to be used in systems with only a single DMA channel. It is enabled by setting the SDC bit in the Interface Configuration Register. All captures and playbacks take place on the playback channel. Obviously, the AD1846 cannot perform a simultaneous capture and playback in Single-Channel DMA mode.

Playback will occur in single-channel DMA mode exactly as it does in Two-Channel mode. Capture, however, is diverted to the playback channel which means that the capture data request occurs on the PDRQ pin and the capture data acknowledge must be received on the $\overline{\text{PDAK}}$ pin. The CDRQ pin will remain inactive LO. Any inputs to $\overline{\text{CDAK}}$ will be ignored.

Playback and capture are distinguished in Single-Channel DMA mode by the state of the playback enable (PEN) or capture enable (CEN) control bits. If both PEN and CEN are set in Single-Channel DMA mode, playback will be presumed.

To avoid confusion of the origin of a request when switching between playback and capture in Single-Channel DMA mode, both CEN and PEN should be disabled and all pending requests serviced before enabling the alternative enable bit.

Switching between playback and capture in Single-Channel DMA mode does not require changing the PPIO and CPIO bits or passing through the Mode Change Enable state except for initial setup. For setup, assign zeros to both PPIO and CPIO. This configures both playback and capture for DMA. Then, switching between playback and capture can be effected entirely by setting and clearing the PEN and CEN control bits, a technique which avoids having to enter the Mode Change Enable state.

DMA Timing

Below, timing parameters are shown for 8-Bit Mono Sample Read/Capture and Write/Playback DMA transfers in Figures 13 and 14. Note that in single-channel DMA mode, the Read/Capture cycle timing shown in Figure 13 applies to the PDRQ and $\overline{\text{PDAK}}$ signals, rather than the CDRQ and $\overline{\text{CDAK}}$ signals as shown. The same timing parameters apply to multibyte transfers. The relationship between timing signals is shown in Figures 15 and 16.

The Host Interrupt Pin (INT) will go HI during the sample period in which the Current Count Register underflows. This event is referenced to the internal sample period clock which is not available externally.

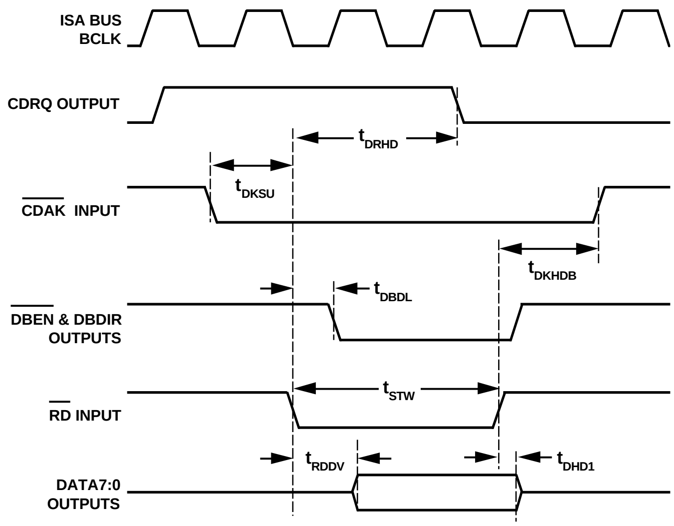


Figure 13. 8-Bit Mono DMA Read/Capture Cycle

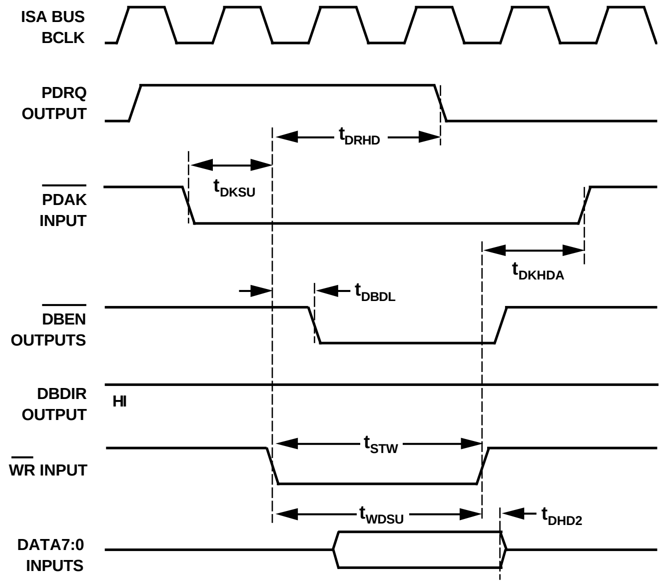


Figure 14. 8-Bit Mono DMA Write/Playback Cycle

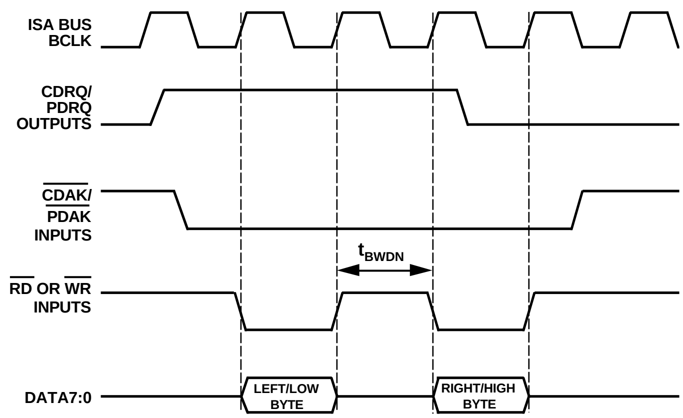


Figure 15. 8-Bit Stereo or 16-Bit Mono DMA Cycle

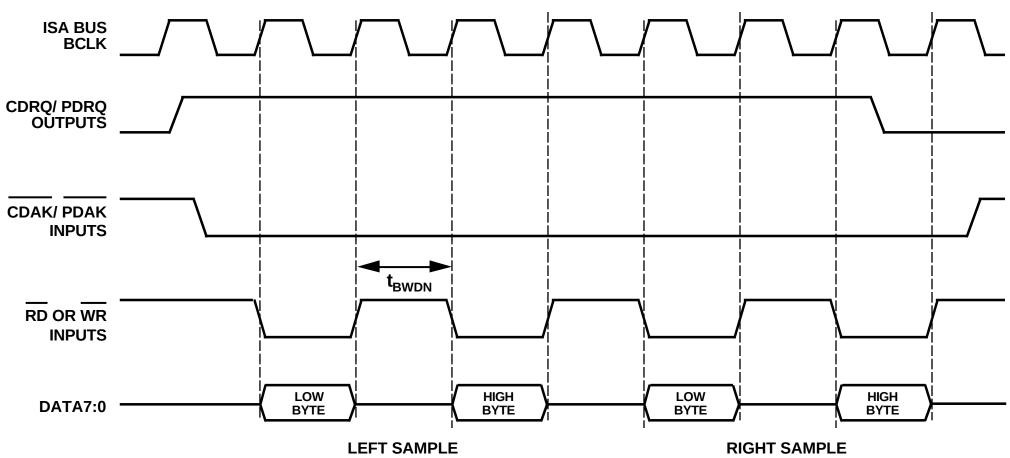


Figure 16. 16-Bit Stereo DMA Cycle

DMA Interrupt

Writing to the internal 16-bit Base Count Register sets up the count value for the number of *samples* to he transferred. Note that the number of bytes transferred for a given count will be a function of the selected global data format. The internal Current Count Register is updated with the current contents of the Upper and Lower Base Count Registers when a write occurs to the Upper Base Count Register.

The Current Count Register cannot be read by the host. Reading the Base Count Registers will only read back the initialization values written to them.

The Current Count Register is decremented every sample period when either the PEN or CEN bit is enabled and also either the Transfer Request Disable (TRD) bit or the Interrupt Status (INT) bit is zero. An interrupt event is generated after the Current Count Register is zero and an additional playback sample is transferred. The INT bit in the Status Register always reflects the current internal interrupt state defined above. The external INT pin will only go active HI if the Interrupt Enable (IEN) bit in the Interface Configuration Register is set. If the IEN bit is zero, the external INT pin will always stay LO, even though the Status Register's INT bit may be set.

POWER UP AND RESET

The $\overline{\text{PWRDWN}}$ pin should be held in its active LO state when power is first applied to the AD1846. Analog Devices recommends waiting one full second after deasserting $\overline{\text{PWRDWN}}$ before commencing audio activity with the AD1846. This will allow the analog outputs to fully settle to the V_{REF} voltage level prior to system autocalibration. At any point when powered, the AD1846 can be put into a state for minimum power consumption by asserting $\overline{\text{PWRDWN}}$ LO. All analog and digital sections are shut down. The AD1846's parallel interface does not function; all bidirectional signal lines are in high impedance state.

Deasserting $\overline{\text{PWRDWN}}$ by bringing it HI begins the AD1846's initialization. While initializing, the AD1846 ignores all writes and all reads will yield "1000 0000 (80h)." At the conclusion of reset initialization, all registers will be set to their default values as listed in "Control Registers" above. The conclusion of the initialization period can be detected by polling the index register for some value other than "1000 0000 (80h)."

It is imperative to autocalibrate on power up for proper operation. See next section.

AUTOCALIBRATION

The AD1846 can calibrate its ADCs and DACs to minimize dc offsets. Autocalibration occurs whenever the AD1846 returns from the Mode Change Enable state and the ACAL bit in the Interface Configuration register has been set. If the ACAL bit is not set, the RAM normally containing ADC and DAC offset compensations will he saved, retaining the offsets of the most recent autocalibration. Therefore, it is imperative to autocalibrate on power up for proper operation.

The completion of autocalibration can be determined by polling the Autocalibrate-In-Progress (ACI) bit in the Test and Initialization Register, which will be set during autocalibration. Transfers enabled during autocalibration do not begin until the completion of autocalibration.

The following summarizes the procedure for autocalibration:

- Mute left and right AUX1 and AUX2 inputs, and digital mix. (It is unnecessary to mute the DAC outputs, as this will happen automatically.)
- Set the Mode Change Enable (MCE) bit.
- Set the Autocalibration (ACAL) bit.
- Clear the Mode Change Enable (MCE) bit.
- The Autocalibrate-In-Progress (ACI) bit will transition from LO to HI within five sample periods. It will remain HI for approximately 384 sample periods. Poll the ACI bit until it transitions from HI to LO.
- Set to desired gain/attenuation values, and unmute DAC outputs (if muted), AUX inputs, and digital mix.

During the autocalibration sequence, data output from the ADCs is meaningless. Inputs to the DACs are ignored. Even if the user specified the muting of all analog outputs, near the end of the autocalibration sequence, analog outputs very close to V_{REF} will be produced at the line output.

CHANGING SAMPLE RATES

To change the selection of the current sample rate requires a Mode Change Enable sequence since the bits which control that selection are in the Clock and Data Format Register. The fact that the clocks change requires a special sequence which is summarized as follows:

- If autocalibration will take place at the end of this sequence, then mute AUX1 and AUX2 inputs and the digital mix.
- Set the Mode Change Enable (MCE) bit.
- In a single write cycle, change the Clock Frequency Divide Select (CFS2:0) and/or the Clock Source Select (CSS).
- The AD1846 now needs to resynchronize its internal states to the new clock. Writes to the AD1846 will be ignored. Reads will produce "1000 0000 (80h)" until the resynchronization is complete. Poll the Index Register until something other than this value is returned.
- Clear the Mode Change Enable (MCE) bit.
- If ACAL is set, follow the procedure described in "Autocalibration" above.
- Poll the ACI bit until it transitions LO (approximately 128 sample cycles).
- Set to desired gain/attenuation values, and unmute DAC outputs (if muted).

APPLICATIONS CIRCUITS

The AD1846 Stereo Codec has been designed to require a minimum of external circuitry. The recommended circuits are shown in Figures 17 through 25. Analog Devices estimates that the total cost of all the components shown in these figures, including crystals but not including connectors, to be less than $10 in the U.S.A. in 10,000 quantities.

See Figure 1 for an illustration of the connection between the AD1846 SoundPort Codec and the Industry Standard Architecture (ISA) computer bus, also known as the "PC-AT bus." Note that the 74_245 transceiver receives its enable and direction signals directly from the Codec. Analog Devices recommends using the "slowest" 74_245 adequately fast to meet all AD1846 and computer bus timing and drive requirements. So doing will minimize switching transients of the 74_245. This in turn will minimize the digital feedthrough effects of the transceiver when driving the AD1846, which can cause the audio noise floor to rise.

Industry-standard compact disc "line-levels" are 2 V rms centered around analog ground. (For other audio equipment, "line level" is much more loosely defined.) The AD1846 SoundPort is a +5 V only powered device. Line level voltage swings for the AD1846 are defined to be 1 V rms for a sine wave ADC input and 0.707 V rms for a sine wave DAC output. Thus, 2 V rms input analog signals must be attenuated and either centered around the reference voltage intermediate between 0 V and +5 V or ac-coupled. The V_{REF} pin will be at this intermediate voltage, nominally 2.25 V. It has limited drive but can be used as a voltage offset to an op amp input. Note, however, that dc-coupled inputs are not recommended, as they provide no performance benefits with the AD1846 architecture. Furthermore, dc offset differences between multiple dc-coupled inputs create the potential for "clicks" when changing the input mux selection.

A circuit for 2 V rms line-level inputs and auxiliaries is shown in Figure 17. Note that this is a divide-by-two resistive divider. The input resistor and 560 pF capacitor provides the single-pole of anti-alias filtering required for the ADCs. If line-level inputs are already at the 1 V rms levels expected by the AD1846, the resistors in parallel with the 560 pF capacitors can be omitted.

The circuit shown in Figure 17 will produce gain/attenuation step sizes for the auxiliary inputs which are a function of the programmed gain/attenuation.

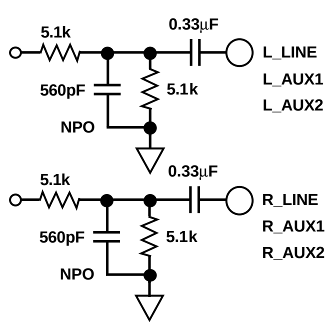


Figure 17. 2 V rms Line-Level Input Circuits

Figure 18 illustrates one example of how an electret condenser mike requiring phantom power could be connected to the AD1846. V_{REF} is shown buffered by an op amp; a transistor like a 2N4124 will also work fine for this purpose.

Particular system requirements will depend upon the characteristics of the intended microphone.

Note that if a battery-powered microphone is used, the buffer and R_2s are not needed. The values of R_1, R_2s, and C should be chosen in light of the mic characteristics and intended gain. Typical values for these might be R_1 = 20 kΩ, R_2 = 2 kΩ, and C = 220 pF.

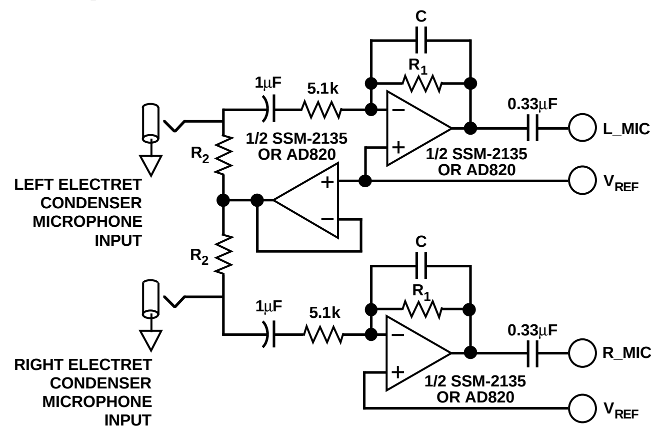


Figure 18. "Phantom-Powered" Microphone Input Circuit

Figure 19 shows ac-coupled line outputs. The resistors are used to center the output signals around analog ground. If dc-coupling is desired, V_{REF} could be used with op amps as mentioned previously.

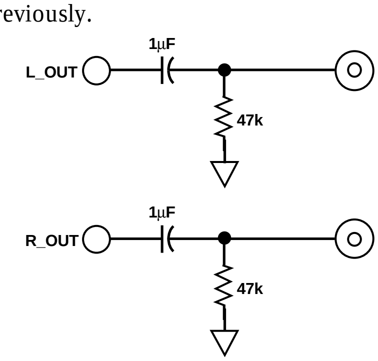


Figure 19. Line Output Connections

A circuit for headphone drive is illustrated in Figure 20. Drive is supplied by +5 V operational amplifiers. The circuit shown ac couples the line output to the headphones.

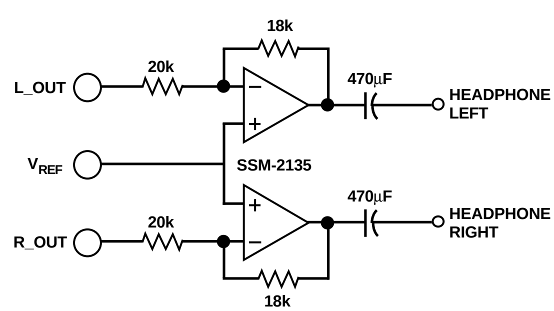


Figure 20. Headphone Drive Connections

Figure 21 illustrates reference bypassing. V_{REF}_F should only be connected to its bypass capacitors.

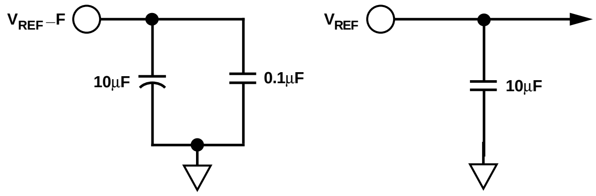


Figure 21. Voltage Reference Bypassing

Figure 22 illustrates signal-path filtering capacitors, L_FILT and R_FILT. The 1.0 µF capacitors required by the AD1846 can be of any type. Note that AD1846s will perform satisfactorily with 0.1 µF capacitors; however, low frequency performance will be degraded.

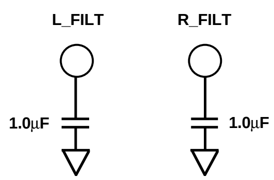


Figure 22. External Filter Capacitor Connections

The crystals shown in the crystal connection circuitry of Figure 23 should be fundamental-mode and parallel-tuned. Note that using the exact data sheet frequencies is not required and that external clock sources can be used to drive the crystal inputs. (See the description of the CFS2:0 control bits above.) If using an external clock source, apply it to the crystal input pins while leaving the crystal output pins unconnected. Attention should be paid to providing low jitter external input clocks.

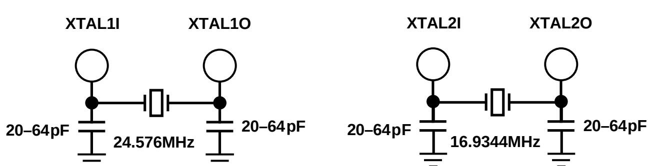


Figure 23. Crystal Connections

Low cost ceramic resonators may be substituted for the crystals to supply the time base to the AD1846.

Analog Devices recommends a pull-down resistor for $\overline{\text{PWRDWN}}$.

Good, standard engineering practices should be applied for power supply decoupling. Decoupling capacitors should be place as close as possible to package pins. If a separate analog power supply is not available, we recommend the circuit shown in Figure 24 for using a single +5 V supply. This circuitry should be as close to the supply pins as is practical.

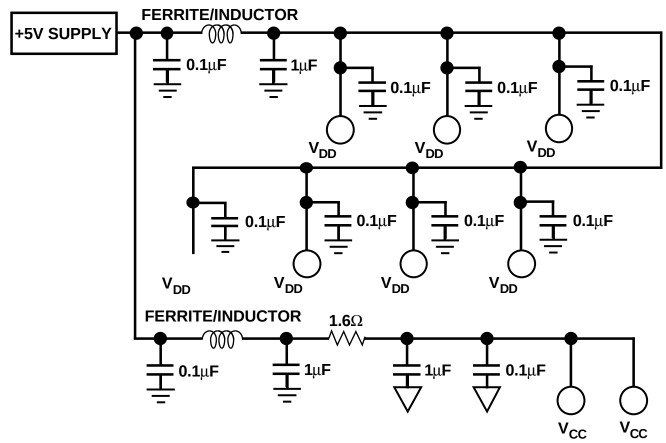


Figure 24. Recommended Power Supply Bypassing

Analog Devices recommends a split ground plane as shown in Figure 25. The analog plane and the digital plane are connected directly under the AD1846. Splitting the ground plane directly under the SoundPort Codec is optimal because analog pins will be located above the analog ground plane and digital pins will be located directly above the digital ground plane for the best isolation. The digital ground and analog grounds should be tied together in the vicinity of the AD1846. Other schemes may also yield satisfactory results. If the split ground plane recommended here is not possible, the AD1846 should be entirely over the analog ground plane with the 74_245 transceiver over the digital plane.

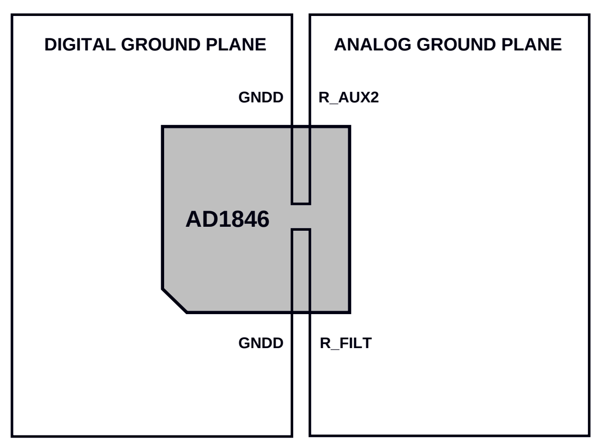
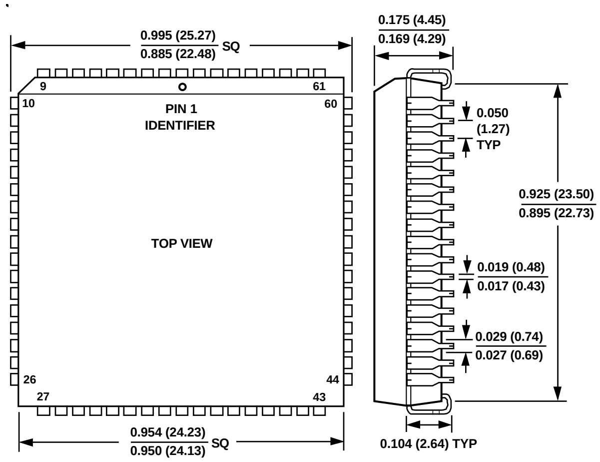


Figure 25. Recommended Ground Plane

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

P-68A
68-Lead Plastic Leaded Chip Carrier



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